Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Previously Presented) A memory device as claimed in claim 21, wherein the piezoelectric material is a ferroelectric material.

3-5. (Canceled)

6. (Previously Presented) A memory device as claimed in claim 21,

the plurality of first electrodes being arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of second electrodes being arranged parallel to each other in a spaced apart manner in a second plane, and

the plurality of third electrodes being arranged parallel to each other in a spaced apart manner in a third plane,

the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first electrodes and the plurality of third electrodes being perpendicular to the plurality of second electrodes.

7-16. (Canceled)

17. (Previously Presented) A memory device as claimed in claim 24,

the plurality of first electrodes being arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of second electrodes being arranged parallel to each other in a spaced apart manner in a second plane, and

the plurality of third electrodes being arranged parallel to each other in a spaced apart manner in a third plane,

the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first electrodes and the plurality of the third electrodes being perpendicular to the plurality of second electrodes.

18. (Previously Presented) A memory device as claimed in claim 25,

the plurality of first electrodes being arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of second electrodes being arranged parallel to each other in a spaced apart manner in a second plane, and

the plurality of third electrodes being arranged parallel to each other in a spaced apart manner in a third plane,

the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first and the plurality of third electrodes being perpendicular to the plurality of second electrodes.

19. (Previously Presented) A memory device as claimed in claim 26,

the plurality of first electrodes being arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of second electrodes being arranged parallel to each other in a spaced apart manner in a second plane, and

the plurality of third electrodes being arranged parallel to each other in a spaced apart manner in a third plane,

the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first electrodes and the plurality of the third electrodes being perpendicular to the plurality of second electrodes.

20. (Canceled)

21. (Currently Amended) A memory device comprising:

a plurality of first electrodes;

a plurality of second electrodes;

a plurality of third electrodes; and

a two-dimensional array of memory cells provided corresponding to intersections between the plurality of first electrodes and the plurality of second electrodes and to intersections between the plurality of second electrodes and the plurality of third electrodes; ~~and~~wherein

~~a plurality of comparators, each of which is provided corresponding to a pair of one first electrode of the plurality of first electrodes and one third electrode of the plurality of third electrodes, each of the comparators having a first input and a second input that are connected to the one first electrode and the one third electrode, respectively,~~

each of the memory cells ~~including~~includes a first layer that includes a piezoelectric material and a second layer including a ferroelectric material,

one second electrode of the plurality of the second electrodes ~~being~~is provided between the first layer and the second layer, and

the first layer and the second layer ~~being~~are provided between one first electrode of the plurality of first electrodes and one third electrode of the plurality of third electrodes;

the memory device further comprising:

a plurality of comparators, each of which is provided corresponding to a pair of one first electrode of the plurality of first electrodes and one third electrode of the plurality of third electrodes, one comparator being thereby provided for each row of the memory cells, each of the comparators having a first input and a second input that are directly connected to the one first electrode and the one third electrode, respectively.

22. (Previously Presented) A memory device as claimed in claim 21, the one comparator comparing a first voltage between the one first electrode and the one second electrode with a second voltage between the one third electrode and the one second electrode.

23. (Previously Presented) A memory device as claimed in claim 22,

the plurality of first electrodes being arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of second electrodes being arranged parallel to each other in a spaced apart manner in a second plane, and

the plurality of third electrodes being arranged parallel to each other in a spaced apart manner in a third plane,

the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first electrodes and the plurality of third electrodes being perpendicular to the plurality of second electrodes.

24. (Currently Amended) A memory device comprising:

a plurality of first electrodes;

a plurality of second electrodes that intersect the plurality of first electrodes;

a plurality of third electrodes that intersect the plurality of second electrodes;

a plurality of memory cells that include a plurality of first layers, each of which includes a piezoelectric material, and a plurality of second layers, each of which includes a ferroelectric material; and

a plurality of comparators, each of which is provided corresponding to a pair of one first electrode of the plurality of first electrodes and one of the plurality of third electrodes, one comparator being thereby provided for each row of the memory cells, each of the plurality of comparators having a first input and a second input that are directly connected to the one first electrode and the one third electrode, respectively;

one first layer of the plurality of first layers being provided between the one first electrode and one second electrode of the plurality of second electrodes, and

one second layer of the plurality of ~~first~~second layers being provided between the one second electrode and the one third electrode.

25. (Previously Presented) The memory device as claimed in claim 24,

one memory cell of the plurality of memory cells being provided between the one first electrode and the one third electrode.

26. (Previously Presented) The memory device as claimed in claim 24,

each of the plurality of comparators being arranged for one of the plurality of pairs of the plurality of first electrodes and the plurality of third electrodes.

27. (Previously Presented) The memory device as claimed in claim 24,

each of the plurality of comparators having a first input that is coupled to one first electrode of one pair of the plurality of first electrodes and the plurality of third electrodes and a second input that is coupled to the one third electrode of the one pair.

28. (Previously Presented) The memory device as claimed in claim 27,

one of the plurality of comparators comparing a first voltage between the one first electrode and the one second electrode with a second voltage between the one third electrode and the one second electrode.

29. (Previously Presented) The memory device as claimed in claim 27,

the plurality of first electrodes being arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of second electrodes being arranged parallel to each other in a spaced apart manner in a second plane, and

the plurality of third electrodes being arranged parallel to each other in a spaced apart manner in a third plane,

the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first electrodes and the plurality of the third electrodes being perpendicular to the plurality of second electrodes.

30. (Previously Presented) The memory device as claimed in claim 28,

the plurality of first electrodes being arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of second electrodes being arranged parallel to each other in a spaced apart manner in a second plane, and

the plurality of third electrodes being arranged parallel to each other in a spaced apart manner in a third plane,

the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first electrodes and the plurality of the third electrodes being perpendicular to the plurality of second electrodes.